THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

Report #1

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Thin-Film Intracortical Recording Microelectrodes

Summary

As we have begun this new contract, we have focused our efforts on finalizing the development of technology needed for high-yield active probe structures. We are examining four structural variations for the formation of Ir/Ti recording sites. The first is the self-aligned single-mask structure used originally. This structure produces a small site and maintains a simple process but does not allow cleaning of the site prior to metallization and is thus prone to problems with adhesion and electrical surface barriers. A second approach involves two masks, cutting through the upper portion of the encapsulating dielectric stack with a dry etch and then following this with a wet etch. The metal is inlayed using a second (larger) mask after an intermediate cleaning step to remove any polymer residue from the surface. This solves the polymer problems but the sidewall of the dielectric opening is irregular due to the different dielectric materials and can lead to step coverage problems. Finally, a third approach cuts through the upper dielectrics to the polysilicon interconnects with a dry etch, deposits the final oxide insulation (LTO), and then opens the contacts through this final layer with a wet etch and a smaller mask. This appears to overcome both the polymer and the step coverage problems and will be evaluated in a study to be conducted during the coming term. The goal is to realize reproducible sites that are free from all of the intermittent problems experienced in the past.

We are also focusing on the development of a series of active 2D and 3D probes as the forerunner of larger arrays to be developed under this contract. The present probes contain one and two-stage unity-gain buffers, amplifiers, multiplexers, and closed-loop "operational" amplifiers configured in a unity-gain mode. Past problems associated with circuit contact resistances appear to have been overcome through work in process development. Metal-silicon contact resistances are now less than 5Ω for all contact combinations (metal-poly, pads, metal-bulk). The new probes have been successfully encapsulated using LTO films deposited in our laboratory, and all designs have been found fully functional with circuit performance close to design targets. For active 3D structures, the problem of protecting the circuit areas from the final probe separation etch while allowing the shanks and 3D mounting "wings" to etch all the way down to the boron etch-stop is an important one. We have successfully used a back etch mask for this purpose, and working probes have been produced. During the coming term, we plan on completing the testing of these probes, both in-vitro and in-vivo.

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should also be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the probe output leads, both in terms of their number and their encapsulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the megohm impedance levels of the sites while maintaining lead flexibility.

Our solution to this problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of about 300, impedance levels are reduced by four orders of magnitude, and the probe requires only three leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

We have launched this new contract with efforts in several areas: 1) we have examined various options for recording site fabrication, ranging from one-mask self-aligned structrures to three-mask structures offering improved control over sidewall profiles and better pre-metallization cleaning ability; 2) we have continued to explore the acute and chronic recording performance of our passive probes; and 3) we have designed and fabricated a new family of active recording probes containing buffers, amplifiers, and multiplexers for simple 2D and 3D recording applications. The results in each of these areas are discussed in the sections below.

2. *Passive Probe Fabrication*

2.1 Site Formation

As has been discussed in previous reports for both recording and stimulation, the formation of reliable sites continues to be an intermittent problem. This problem has surfaced in various ways: poor adhesion of sites and bonding pads, open-circuit sites, EDP attack of the polysilicon conductors under the sites, and abnormal site electrochemical characteristics. The source of the problem has been traced to a number of causes, including polymer formation in the contacts during dry etching (RIE) and poor step coverage of the metal. The intent of this section is to summarize the options for site formation, to discuss the benefits and drawbacks with each one, and to outline a plan for characterization so that we may choose the most reliable technique.

The four basic methods which we have or will evaluate for site formation are shown in Fig. 1. Our original process used RIE to open the dielectrics and, using the same photoresist mask, liftoff subsequently deposited metal to form a metal inlay in the site and bonding pad areas. This was a simple single-mask process which worked well for at least several years. However, increasingly frequent occurances of electrically-open sites and peeling or bubbled metal such as that shown in Fig. 2 indicated a problem. The source of this problem was linked to surface contamination (fluorocarbons) in the opened site areas left by the RIE process prior to metal sputtering.

The second approach, which we currently use, utilizes two masks to form the sites. RIE is used to partially open contact vias (almost through the lowest oxide layer) using a small mask. A wet etch through the same small mask is then used to finish the etch and remove surface contaminants. A second larger mask is finally used to deposit the metal and define the site area. The benefits offered by this technique are that it permits vigorous cleaning of the contact openings prior to metal deposition, and that it allows the sites to overlap adjacent conductors permitting higher site densities without adding shank width (Fig. 3). The disadvantage is that there is potential for a step coverage problem, both over the top edge of the stacked dielectrics and over the nitride "shelf" which forms during the wet etching/cleaning step.

Electrochemical tests on sites formed using the second approach (see "Micromachined Stimulating Electrodes Quarterly Report #6, April 1997) carried out by Drs. Heetderks and Schmidt at NIH, and by EIC Labs, indicate that this may indeed be the case. Negative open circuit potentials of the sites and deviant impedance spectra indicate the existence of an alternate current path from the electrolyte to the polysilicon conductor other than iridium. There is now some evidence that this problem was restricted to one sputtering run in which the abnormalities can be attributed to contamination of the iridium target used for this given run. Indeed, about the time that these probes were fabricated the iridium target was sputtered away over a portion of its area, exposing (and likely depositing) the solder backing layer. We discovered this problem a few weeks later and have since switched to our backup iridium target. (We need to purchase a new backup, since target acquisition takes several months.) We are still trying to confirm that this is the cause of the abnormal site behavior and intend on doing elemental analysis on the affected sites during the next few weeks.

Recent SEMs of sites formed using the second approach in multiple sputtering runs, however, still indicate a potential structural problem. Figure 4 shows a high magnification SEM of one of the 3μm vias used to contact the polysilicon. While a cross-

section of this structure would be more definitive and we intend to study this further, there is evidence of several discontinuities in the iridium.

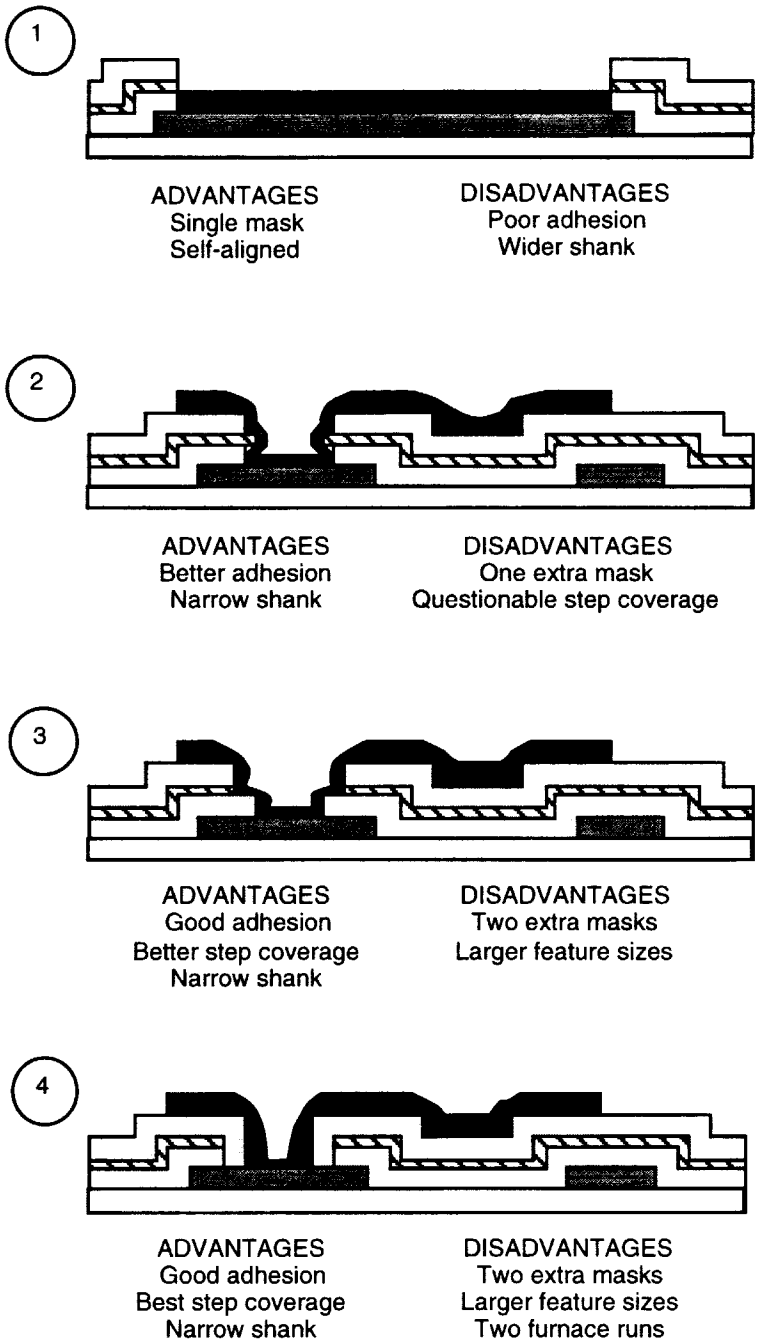


Fig. 1: Four options for electrode site formation. The first is a single-mask self-aligned process. The second requires two masks but has the added advantage of including an intermediate cleaning step. The third and fourth methods require yet another mask (three in total) but are more foolproof in terms of step-coverage. In the fourth technique the upper oxide dielectric is deposited after opening the contact vias down to the polysilicon and the final etch can be performed wet.

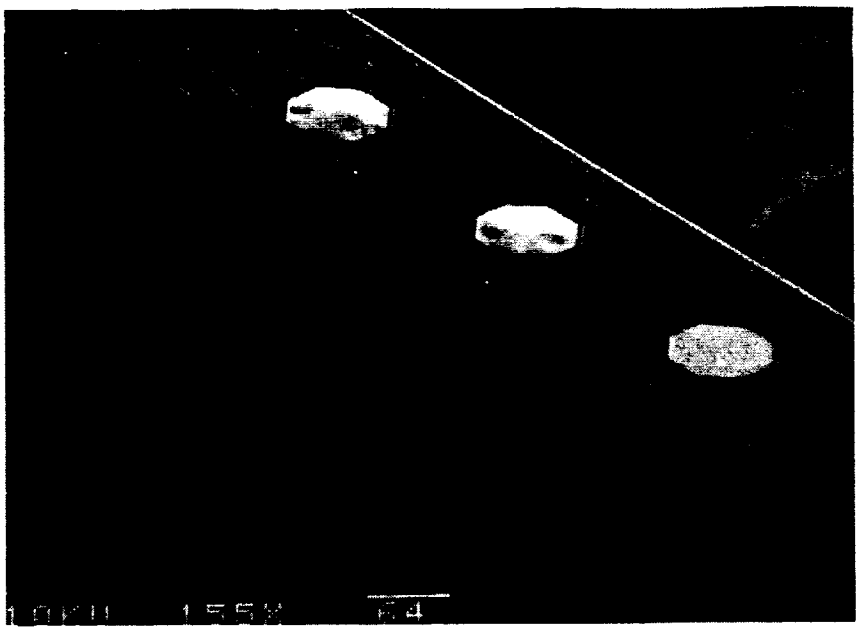


Fig. 2: Example of bubbled sites sometimes seen with self-aligned site formation, the original method used. The cause of poor adhesion was traced to surface contaminants between the metal and the underlying polysilicon.

While it certainly appears at this time that the second approach is not optimal for site formation, it is still not clear that its inherent difficulties cannot be overcome. For instance, a thinner lower oxide would reduce the adverse effects of the nitride shelf. It may even be possible to eliminate the lower oxide layer altogether along with increasing the thickness of the top oxide for stress compensation. We intend to investigate these alternatives along with the more complex third and fourth approaches to be described below.

The third and fourth approaches outlined in Fig. 1 involve three masking steps to realize a site. In the third method, the upper oxide and nitride are removed using wet and/or dry etching with a larger mask. A smaller mask is then used to open the lower oxide with a wet etch. Finally, an even larger mask is used to deposit the metal and define the site area. This method has several advantages. It can be done completely with wet etching which eliminates the RIE surface contamination problem. As with the second approach, leads can be routed under sites to conserve probe width. The main disadvantage is that an additional masking step is needed, increasing passive probe fabrication to an eight mask process. Another drawback is that the minimum feature permitted to define a site is increased by several microns due to the need for additional alignment tolerances. These are small tradeoffs, however, if the enhanced process yields reliable contacts.

The fourth proposed method also involves three masking steps. Here, the lower two dielectrics (oxide and nitride) are first deposited and etched using wet and/or dry etching. The upper oxide (e.g., LTO) is then deposited and a smaller mask is used to open the contact using a wet etch. In this way, the sidewalls of the upper oxide conformally smooth the outer dielectric cuts, resulting in a better step transition eliminating the nitride shelf seen in method #2. The actual contact vias are opened through this oxide and can be formed using a wet etch. This approach similar to the third method except that the initial dielectric etch can be taken down to the polysilicon (eliminating any critical timing and any

effects of etch anisotropy on the sidewall profile). An additional furnace run required to separately deposit the upper oxide.

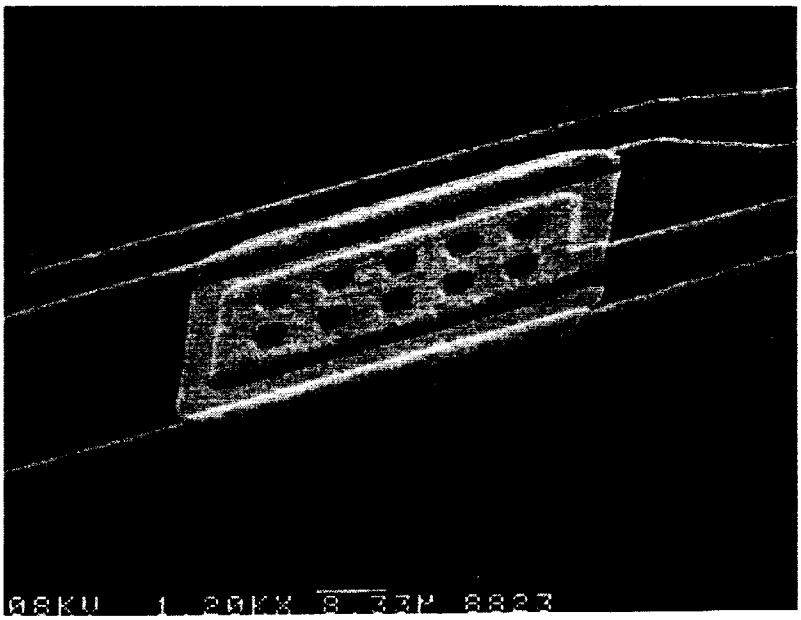


Fig. 3: Example of a site fabricated using the second approach. Here, contact to the underlying polysilicon is formed using 3μm vias. The iridium site is then defined using lift-off with a larger mask. In this way, the site can overlap adjacent leads.

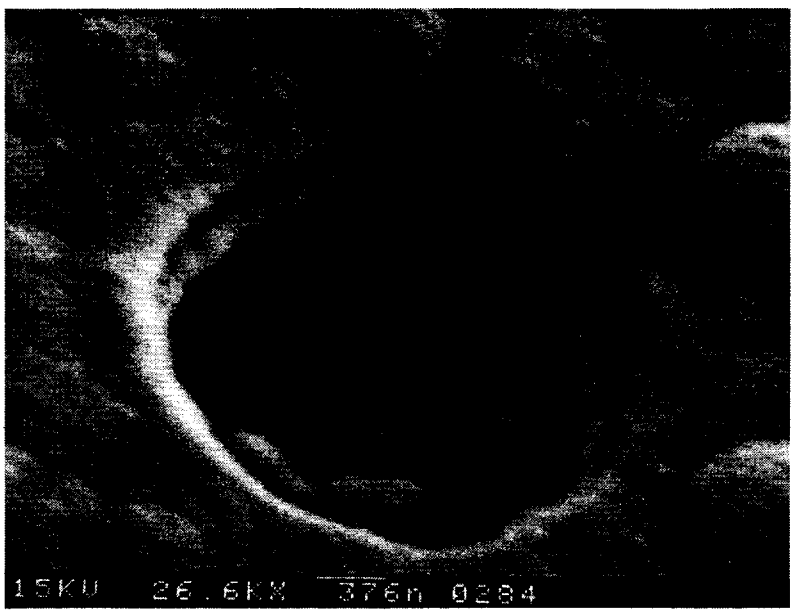


Fig. 4: SEM of a 3μm contact via. Note the apparent discontinuities in the iridium both above and below the nitride shelf.

During the coming reporting period, we will design and fabricate a mask set to test the third and fourth site formation methods. Along with standard recording and stimulating probe designs for post-process testing, various test structures will be included for in-process evaluation of the contacts. These structures, outlined in detail in "Thin-Film Intracortical Recording Microelectrodes" Quarterly Report #6 (May 1995), include contact strings to verify linearity of contacts, railroad track structures to verify metal continuity (step coverage), and Kelvin bridges to measure resistance of individual contacts. We will simultaneously fabricate probes using the second approach so that all devices to be tested will have gone through the same sputtering and furnace runs, permitting a direct comparison of results. Once fabricated, probe sites will be subjected to a battery of electrochemical tests including impedance spectroscopy, open-circuit potential measurement, and cyclic voltammetry. Vigorous optical inspection using SEM is also planned. By summer's end we hope to have determined the best method for fabricating reliable sites.

2.2 Recording Experiments

Through the Center for Neural Communication Technology, we are providing electrodes to Dr. John Middlebrooks at the Kresge Hearing Research Institute here at the University of Michigan. Dr. Middlebrooks is using a 16-channel linear array to investigate the role of neurons in the auditory cortex in sound localization in the cat. Figure 5 shows mean spike counts measured at eight electrode sites in response to noise-burst stimuli presented at five locations in the horizontal plane. The distribution of activity across the electrode array provides a measure of a portion of the "cortical image" of a sound source. Dr. Middlebrooks uses an artifical-neural-network algorithm to recognize cortical images evoked by single stimulus presentations and, thereby, estimate the location of the sound source. Additional experiments in the Middlebrooks lab involve studies of the coding of sound-source location by the relative timing across multiple recording sites.

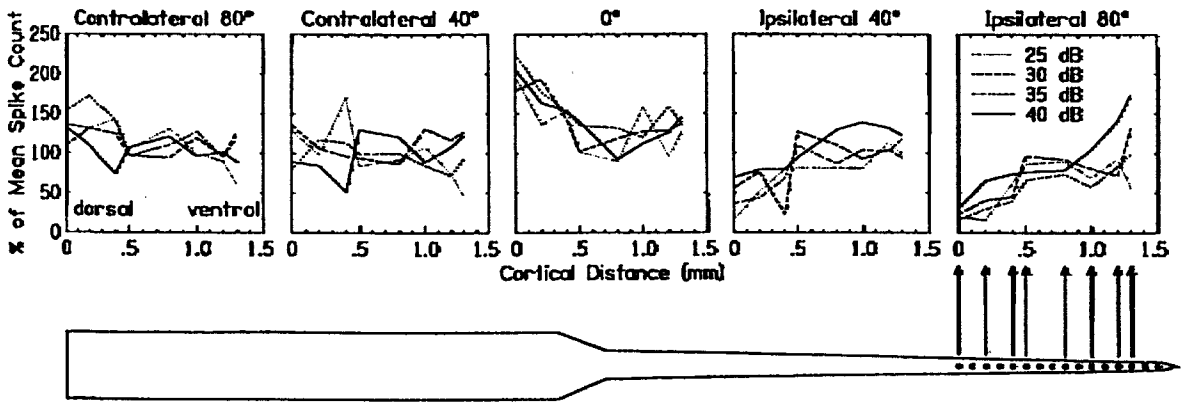


Fig. 5: Data obtained by Dr. John Middlebrooks from cat auditory cortex in response to noise-burst stimuli presented at five locations in the horizontal plane. The distribution across the linear electrode array provides a measure of a portion of the "cortical image" of a sound source.

The preliminary experiments have used an available electrode design, but Dr. Middlebrooks plans to design an electrode that will permit optimal simultaneous sampling of cortical images across about 3mm of cortex.

One of the major difficulties we have had with chronic microprobes has been their interface with the brain. We have seen electrodes become broken due to fibrous tissue growth, migrate into or out of the neural tissue, and become encapsulated with reactive tissue. In an attempt to achieve better integration between the surrounding neural tissue and the probes, we have begun to look at biopolymer coatings of the neuroprobes. These biopolymer coatings may help by providing anchors for neural tissue to grab onto; they may also be used to deliver chemical substances directly to the tissue or even prevent tissue from attaching to the electrodes where it is not wanted. These biopolymer coatings are being developed by Dr. David Martin here at the University of Michigan under a separate NIH contract and in collaboration with the Center for Neural Communication Technology.

We have implanted 4x4 3-D electrode arrays into guinea pig cortex in three animals. Each guinea pig received two electrodes, one on each side of the brain. The electrodes implanted into the left side of the cortex were dip-coated with 10 mg/ml of SLPF (silk-like protein with fibronectin) in formic acid. The electrodes on the right side were dip-coated with 10 mg/ml SELP5 (silk-like protein with elastin) in formic acid. The electrodes will remain implanted for a period of three weeks after which the animals will be sacrificed and the tissue harvested for histological evaluation. We will also implant an additional three animals with two other coatings and report on these as well.

We will use the EXAKT sectioning method to examine the neuroprobe/brain interface and will report on these findings in the next progress report. The EXAKT tissue sectioning method is a technique which allows us to leave the neuroprobes in place within the brain and section through them with a diamond band saw. This also allows us to obtain 3-D views using the confocal microscope. We believe that this will allow us to gain a better understanding of the brain/probe interface than previously obtained.

3. Active Three-Dimensional Recording Probe Arrays

Microassembling two-dimensional planar probes to create three-dimensional probe arrays has been a primary research focus at Michigan because it allows us to combine all of the features of 2D passive and active probes (multiple sites, laterally and in depth; variable shank widths, lengths and shapes; ribbon cable interconnects; and built-in circuitry for multiplexing and signal processing) in arrays that are capable of interfacing with 3D blocks of neural tissue. We have successfully developed a microassembly structure using electroplated beam leads on the probes to form the orthogonal lead transfers. The gold beams are bent at right angles and attached to the pads on the supporting platform using wire-free bonding. The approach is relatively easy and robust with high yield. We feel this technology is ready to support 3D arrays up to at least 16x16 shanks and 1024 sites. However, even with silicon ribbon cables, bringing out more than a hundred leads from a passive 3D probe is impractical. On-chip circuitry is mandatory to reduce the external leads by multiplexing the recording channels and/or selecting sites close to the active neurons. We can also build on-chip amplifiers to boost the signal-to-noise levels. Such amplifiers would also reduce the electrode output impedances far below their megohm levels via output voltage buffers in order to minimize externally-induced noise/crosstalk and reduce the performance demanded of the encapsulating dielectrics in chronic implant situations. At Michigan, we have been developing multichannel (2D) active probes for several years. We have developed fabrication process for 2D active probes and gained experience in the

design of on-chip recording/stimulating circuitry and external systems. All these form a solid foundation for developing active 3D recording probe arrays.

We have recently designed a new set of active recording probes, some of which can be assembled into 3D arrays. Each probe design tests a certain basic circuit block, including buffers, amplifiers, and 4:1 multiplexers. Our goal is to evaluate these circuit blocks in terms of power consumption, area consumption, noise level, and amplification. We want to address in more detail issues such as DC baseline stability, multiplexer clock noise, and the role of the bias applied to the probe substrate. During the past few months, we have fabricated the first set of these active probes. We have worked to optimize the process flow and have extended the technology to 3D active probe systems. We have now tested some of the probe designs and have obtained results close to the design targets. We plan to finish testing these designs and finalize the fabrication process in the coming months. In addition, we will test these probes in-vivo and finish the evaluation of the probe designs.

3.1 Fabrication of the Active 3D Probes

Although the technologies required for the fabrication 3D passive probe arrays and 2D active probes are fairly well developed, there are new challenges in fabricating active 3D probe arrays. We are now addressing those challenges. We have achieved very low contact resistances on all kinds of contacts with different metals. We have also come up with ideas to solve several step coverage and adhesion problems. We have recently employed a backside alignment step to provide additional protection for the circuit area of the probes during final EDP etching. These areas are discussed below.

Unlike the previous active recording probe process, which uses double polysilicon layers to form capacitors, the process of for active 3D probes employed here uses a single layer of polysilicon along with a shallow boron diffusion layer (primarily used to form ribbon cables and shape probe tips) to form capacitors. In addition, in the new active 3D process, a 400nm-thick layer of HTO has been added to the existing 50nm/120nm oxide/nitride stack (which is used in the LOCOS process to form the active device areas under the polysilicon interconnects. This reduces the capacitance between the probe substrate and the recording electrodes, which will minimize neural signal loss and reduce noise coupling.

Contact resistance has been a significant problem for active probes in the past, and has been primarily responsible for the low yields obtained from probes such as PIA-2, our second-generation 2D 32-site recording array. We have now demonstrated processes for overcoming this difficulty. Great care has been taken to monitor the RIE etch rate using different recipes on different materials and to use probe-tests to determine the etching end point. Piranha cleans (H_2SO_4 : H_2O_2 = 1:1) have then been done as in passive probe processing. A 20-30 sec buffered HF dip just before metal sputtering is necessary for good contacts. A 40nm/600nm Ti/Al(0.5% Si) layer is then sputtered onto the wafer. After lift-off, a 20 minute sintering process at 450°C in a H_2/N_2 ambient is carried out. Circuit contacts to polysilicon, CMOS source/drains, and the p-type substrate are typically around 0.3Ω, 1Ω, and 2Ω (per 3μm x 3μm contact) respectively. Ti/Ir site contacts and Cr/Au pad contacts are also around 1-2Ω per contact.

This has been the first time that we have used our own LTO (425°C) films to passivate the on-chip circuitry. The quality of the LTO has been good, and the uniformity across the wafer is reasonable. However, in subsequent process steps such as Piranha

cleaning, we have noted some attack of the the underlying circuit metal. As shown in Fig. 6, most of this attack occurs at the corners and edges of the metal patterns. When the metal lift-off is not smooth, leaving metal pieces (shown in Fig. 7) at the corners and edges of the patterns, it makes it subject to potential LTO coverage problems. These places are also easily broken in ultrasonic cleaning steps. Ultrasonic cleaning is sometimes necessary when difficult lift-off occurs; however, the associated cleaning time should be kept as short as possible. Figure 8 shows an extreme case where the wafer went through more than 30 minutes of ultrasonic cleaning, which broke/cracked the LTO in many areas. We are not sure whether the adhesion of LTO over LPCVD nitride may also have contributed to this problem. We are going to explore this more and compare the adhesion of LTO over LPCVD oxide (namely HTO) to that over nitride. No matter what the results are, it is clear that a clean metal lift-off is the key to solving the metal undercut problem. We therefore decided to make a clear-field metal mask for the circuit aluminum and use image reversal to form the photoresist patterns. As illustrated in Fig. 9, image reversal generates a negative photoresist profile, which eases lift-off and gives clean metal edges. The reason we usually use normal lithography to pattern for metal lift-off is that image reversal requires two softbakes at different temperatures and two exposures. Image reversal may fail if any of the process conditions (such as ambient temperature, humidity, bake temperature and time, exposure time, or even the photoresist quality itself) is not carefully controlled, especially when there are small features present.

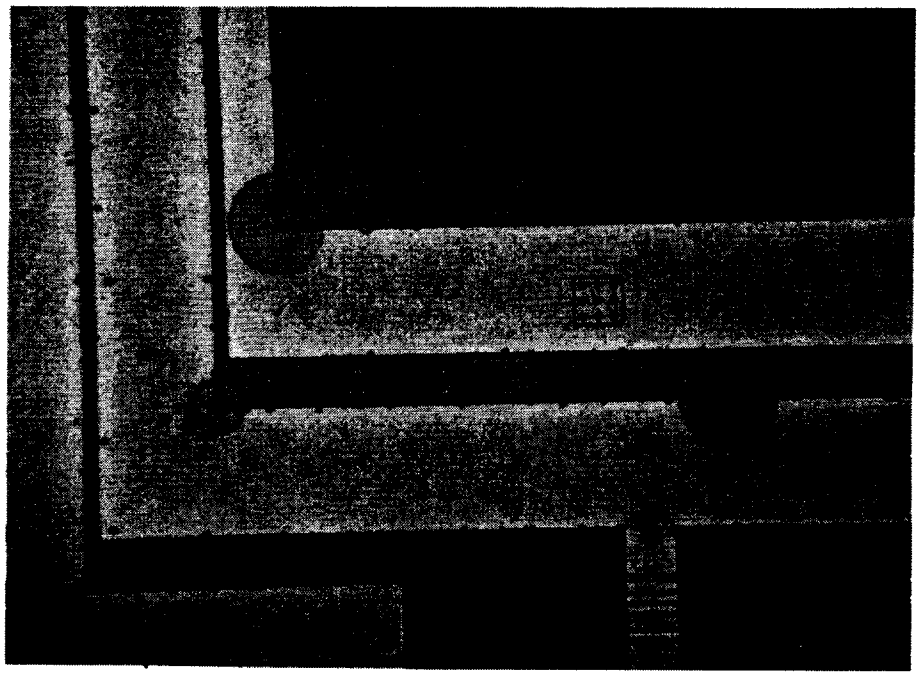


Fig. 6: An example of circuit metal being attacked in the subsequent wet etching/cleaning steps due to LTO coverage problems.

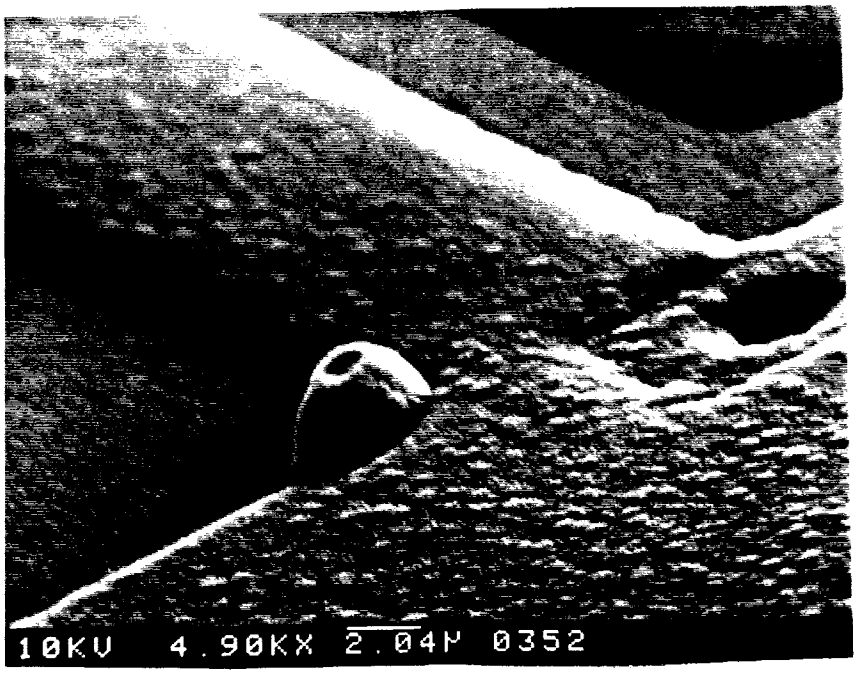


Fig. 7: A metal hillock at the corner of a circuit metal pattern resulting from lift-off. It is the source of potential LTO coverage problems.

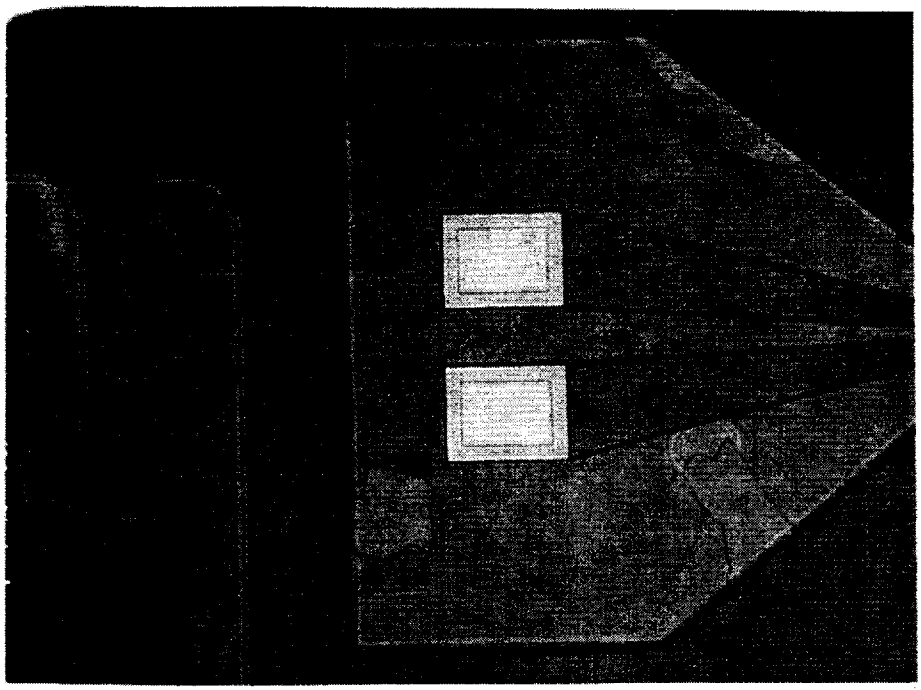
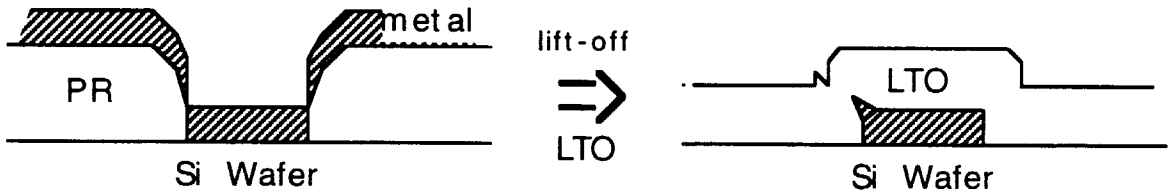
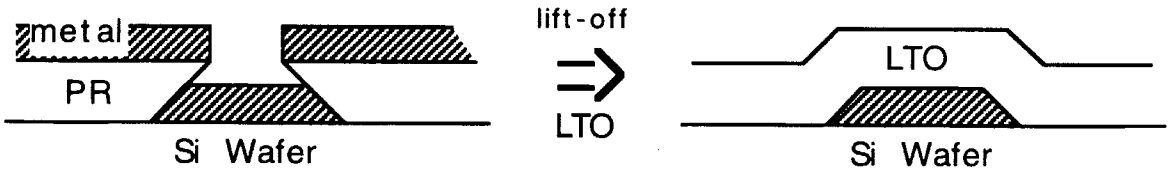


Fig. 8: An example of LTO breaking away from the underlying LPCVD/HTO dielectrics after the wafer went through over 30 minutes of ultrasonic cleaning.

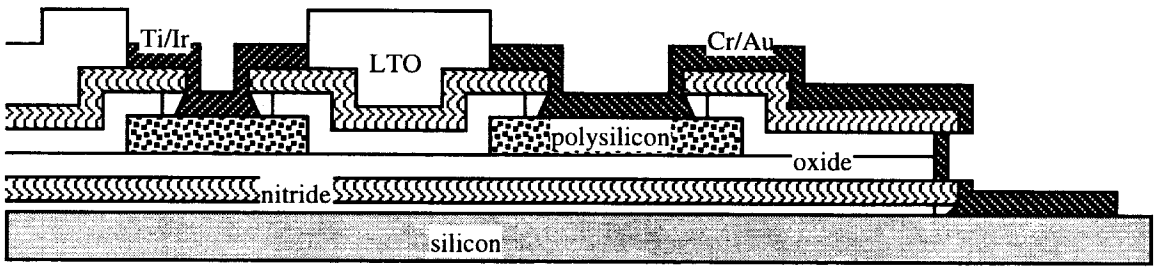


a) Normal lithography and its lift-off

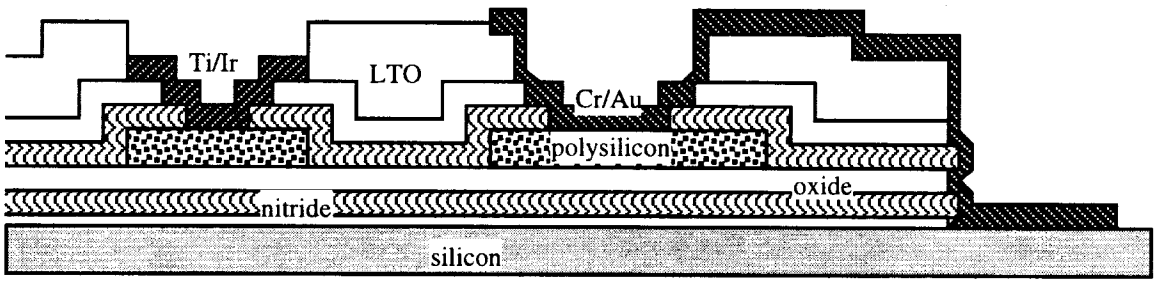


b) Image reversal and its lift-off

Fig. 9: Normal lithography and image reversal generate different photoresist profiles which greatly affect the resulting lift-off step.



a)Using LPCVD oxide/nitride as dielectric between polysilicon and circuit metal could cause step coverage problem



b)Using LPCVD nitride/oxide between polysilicon and circuit metal and an extra mask to open the Au beam contacts would have less step coverage problem.

Fig. 10: The sequences of dielectric layers between polysilicon and circuit metal make a significant difference in the step coverage obtained.

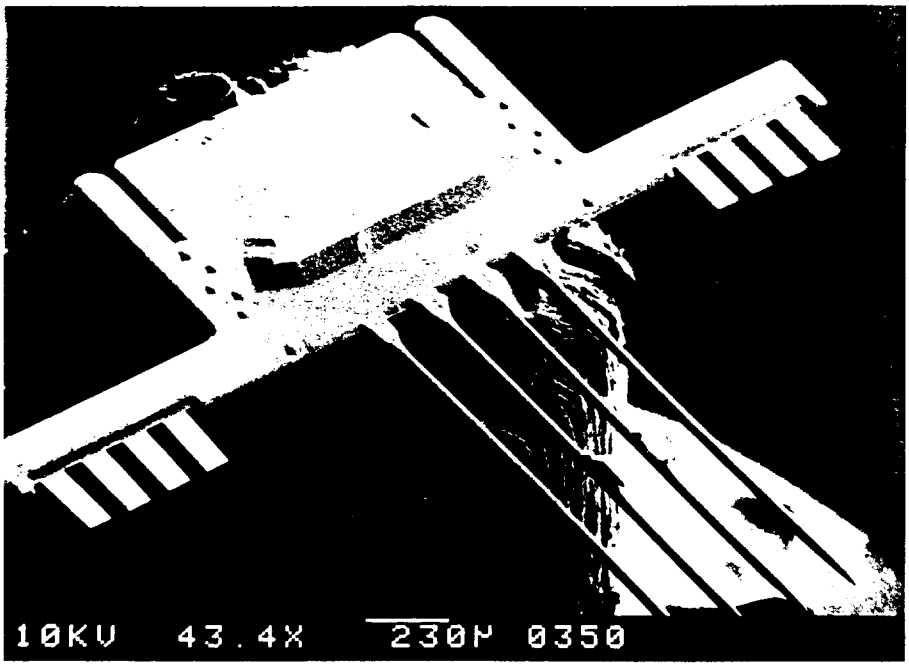
Just as in other probe process sequences, step coverage in the Ir site contacts and between the Au pads/beams and the polysilicon interconnects has been a problem due to the nitride lip resulting from undercutting the lower oxide during BHF etching. This problem has been discussed above along with several solutions. This problem has been helped by interchanging the positions of the LPCVD nitride and oxide layers. Figure 10 shows how this exchange eases the step coverage problem. It may also help the adhesion of LTO as discussed before. For a 3D probe, attention should also be paid to the step coverage of the gold beams over the probe field dielectrics. An extra mask is needed to open the beam/pad contacts so that the time of wet etching can be kept short before putting down Cr/Au.

When we originally designed the mask set for these new active probes, we underestimated the effects of anisotropic EDP etching and put all the probes as close to each other as possible in order to save the area. This resulted in difficulty in etching the active probes out without having the circuit area undercut. Figure 11 shows examples of a failed EDP etch. The probe circuitry has been attacked in EDP, while the shanks are not yet cleared. For 3D active probes, the EDP etch is more critical than that for 2D active probes. Not only must the circuit area not be undercut, but also the probe shanks and platform mounting wings should be etched clear completely down to the p+ etch stop so that the probes can be inserted in the platform slots and spacers will fit in the probe wings. In order to solve this problem, we have added a mask for backside protection. As shown in Fig. 12, it allows us to form Cr/Au patterns on the backside of the wafers to protect the circuit areas. Eight minutes of $HF:HNO_3$ thinning generates about a 90μm difference in height between the circuit areas and the non-circuit areas, which allows us to thin the wafer (non-circuit areas) to less than 70μm while still giving us an hour or so of time tolerance to prevent EDP from undercutting the circuit areas from the back. EDP may still etch the circuit from sides and corners, but since we can finish etching within 40 minutes or less, the chance of having the circuit area undercut from the sides and corners is greatly reduced. Figure 13 shows the finished probes using backside protection. We feel this method can greatly improve the yield of the EDP etch step, especially for 2D active probes. But due to the non-uniform nature of $HF:HNO_3$ thinning, sometimes we still face difficulties in having the probe mounting wings etch clear. One way to resolve this issue is to add 45° slots along the mounting wings so that they will be etched from both the frontside and backside. This has been suggested in our Stimulating Electrode Quarterly Report #6.

We have just finished the fabrication of one of the wafers containing the new probes. Figure 14 shows SEM pictures of the fabricated active probes. Figure 15 shows these active probes on a penny. All the probes have 1.25mm-long shanks with recording sites 1mm below the back portion of the device. The active 3D probes have heights of either 1mm or 0.7mm above the platform, depending on the design.

3.2 Testing of Active 3D Probes

As discussed earlier, the contact resistances of this run of active probes are very low. The transistor characteristics shown in Fig. 16 are also excellent. However, the threshold voltages of both the NMOS and the PMOS transistors are slightly different from their expected values of ±0.85V. The threshold voltage of the NMOS transistor on average is 0.72V. The typical threshold voltage of the PMOS transistor is -1.08V. We believe these differences are mainly because of the higher than expected thermal budget after threshold implant. We have increased the threshold implant doses on some of the wafers that are still being processed and have also tried to minimize the thermal budget by skipping some of the non-critical high temperature steps. We expect the coming active probes to have better threshold voltages.



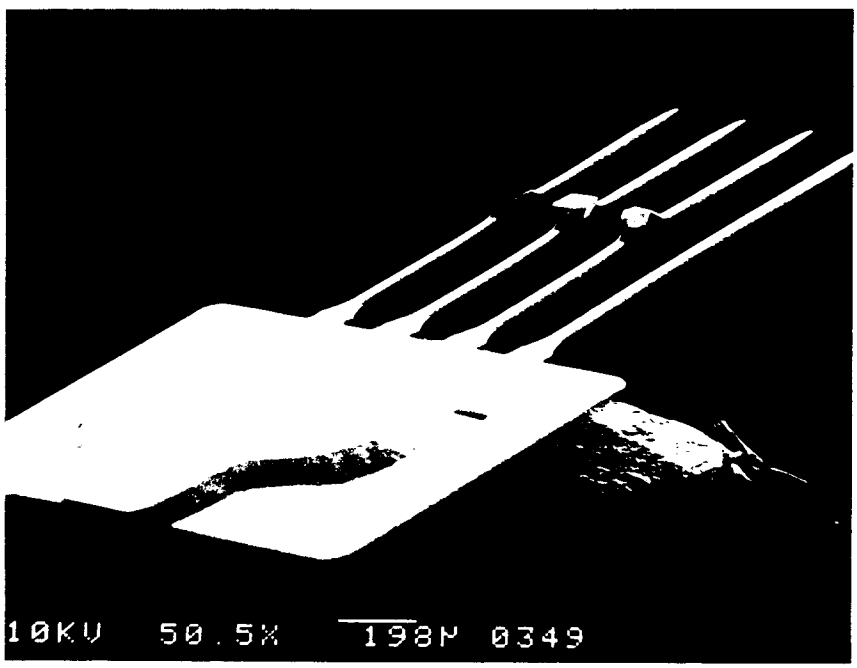
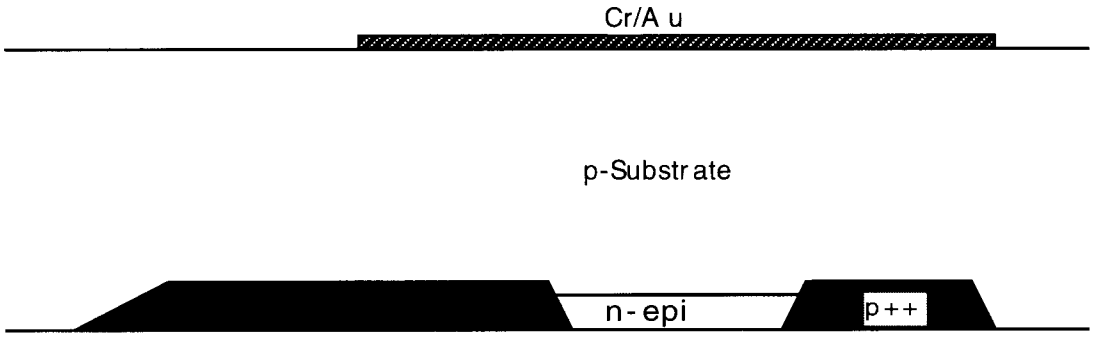
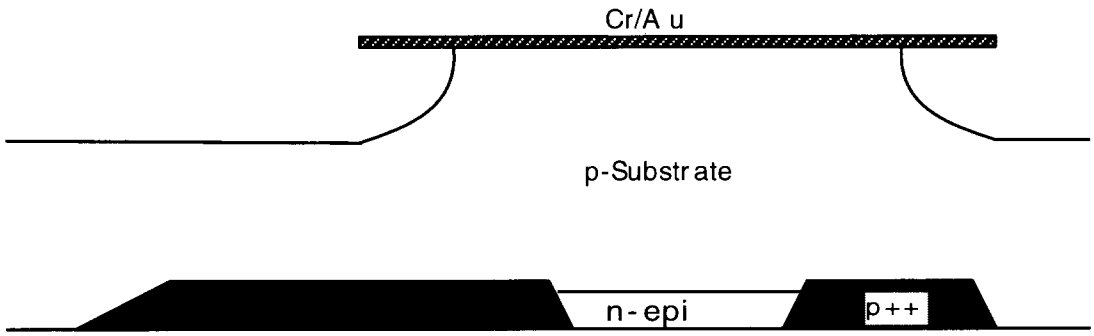


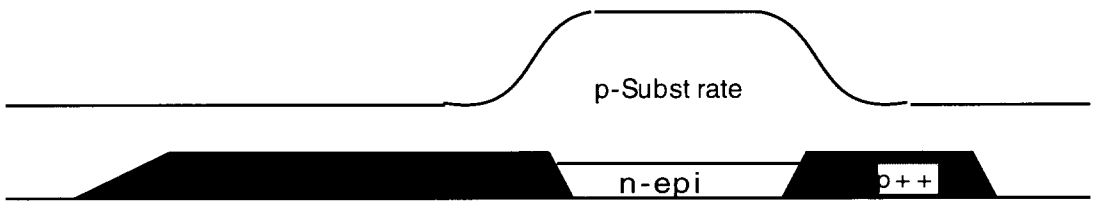
Fig. 11: These SEM photos show 2D and 3D active probes that have had their circuit areas undercut in EDP due to excessive etching from the outer corners of the die while the shanks are not yet free of undoped silicon. In the shank areas, etching from the front side of the wafer proceeded from the probe tips back along the p+ shank and from the base of the shanks (where interleaved shanks from another probe did not extend, leaving a wider area between shanks and a deeper etch) forward. In this case a small bump of silicon remains in the middle of the shanks where the two etch fronts have not quite met.



a)Using backside lithography to form Cr/Au protection over the circuit area



b) About 8 minutes HF:HNO_3 thinning with Cr/Au protection layer



c) Remove Cr/Au layer and continue HF:HNO_3 thinning

d)EDP etch to release the active probes

Fig. 12: Process flow using a backside Cr/Au mask to protect the circuit area during EDP etching.

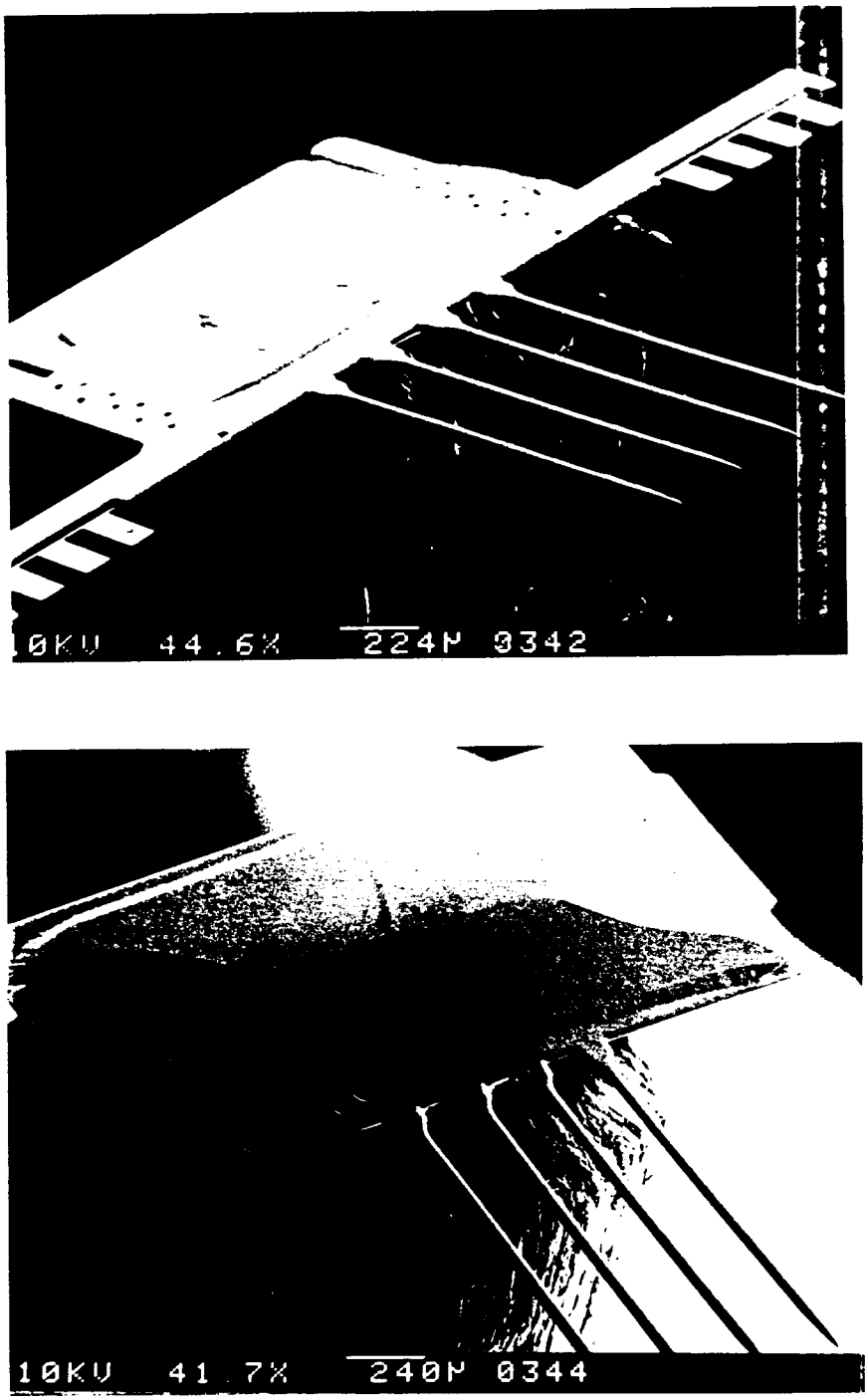


Fig. 13: By using a backside Cr/Au mask, the active probes are well protected in the circuit areas while their mounting wings and shanks are etched clear in the final EDP etch.

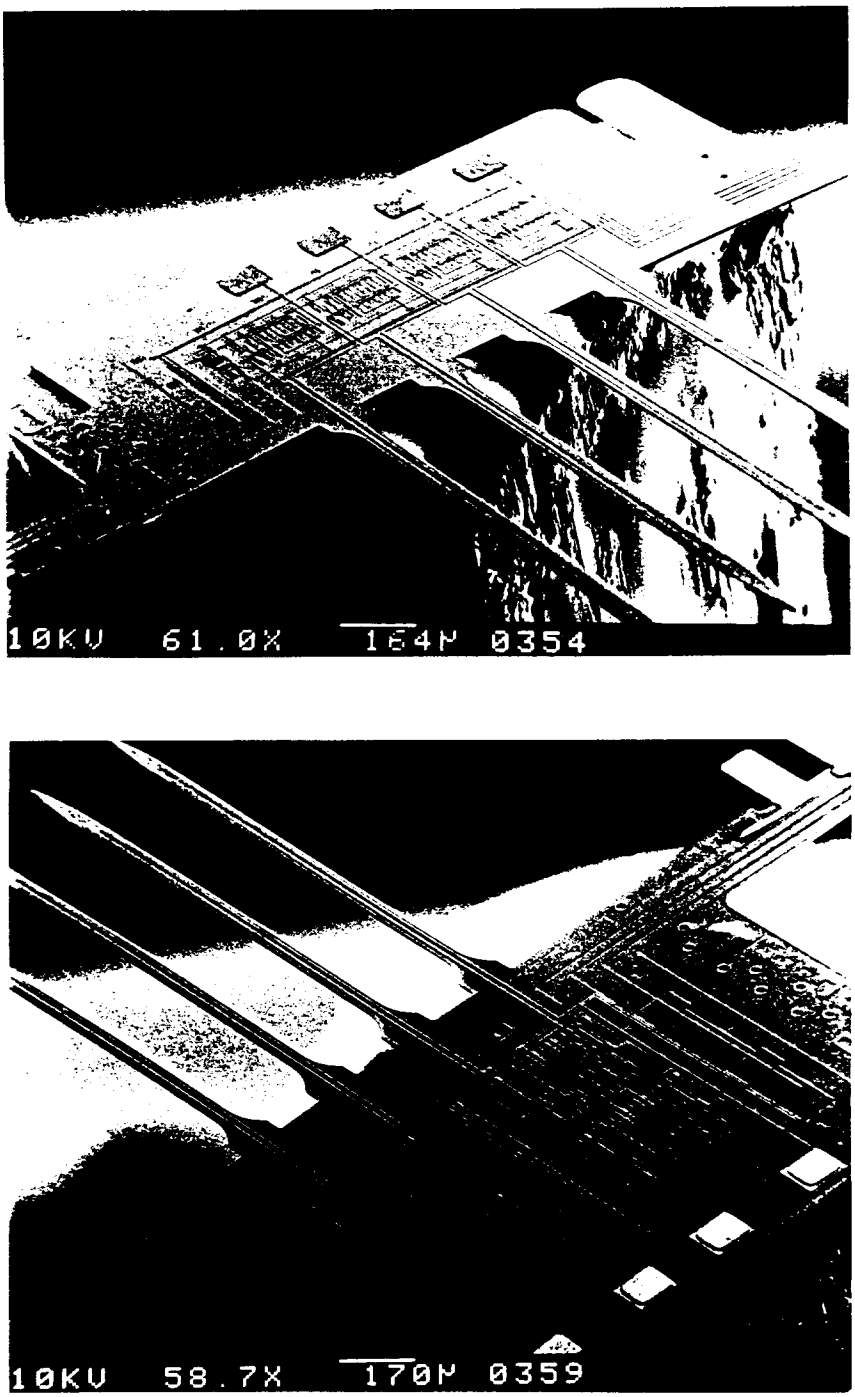


Fig. 14: SEMs of finished active probes. The probes contain amplifiers, buffers, and multiplexers and are the forerunners of more complex PIA-3 probes.

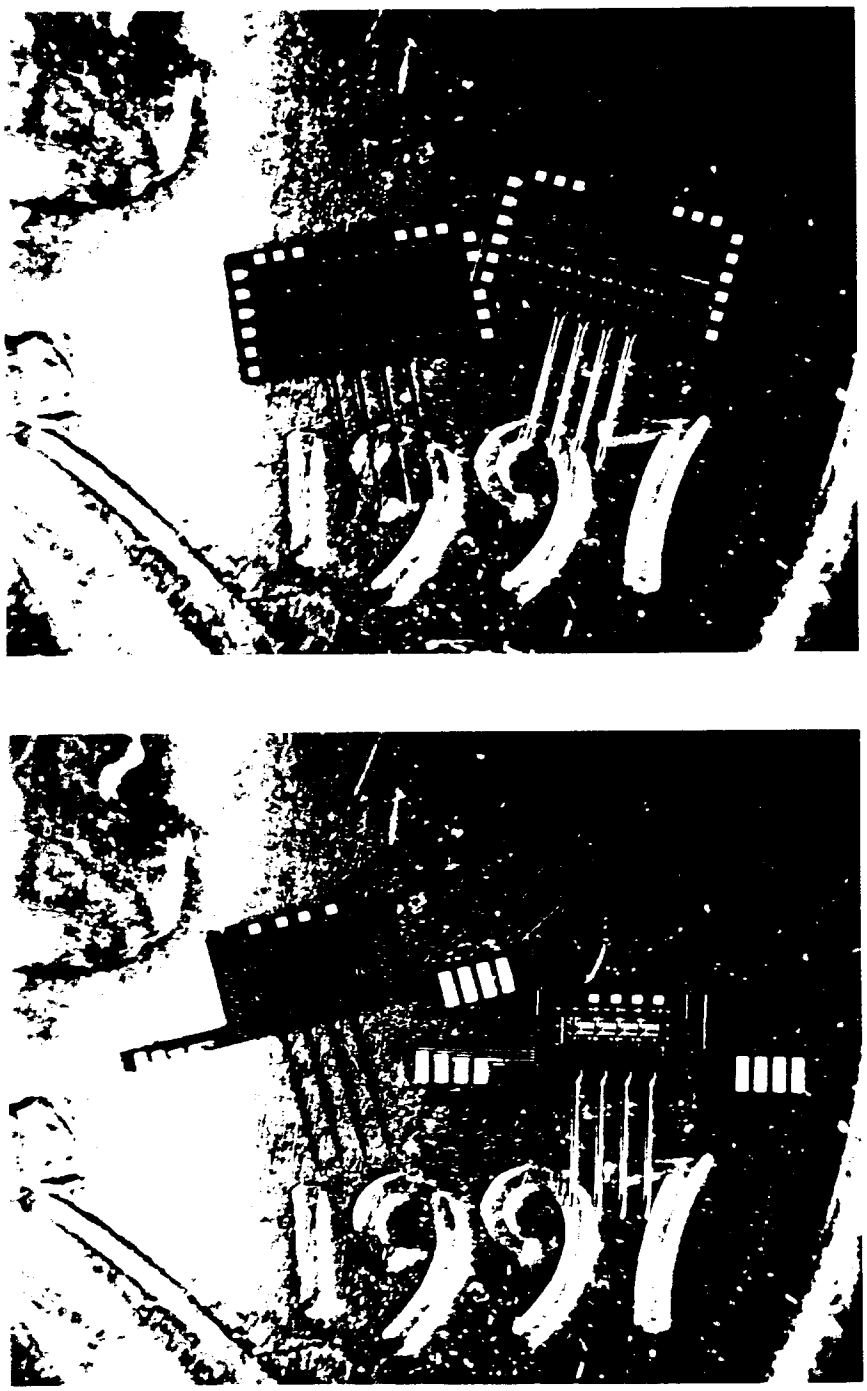


Fig. 15: Active probes shown on a penny for size comparison. The shanks are 1.25mm long overall.

We have tested some of the circuit designs before and after depositing passivating LTO. As expected, the threshold voltages barely changed (typically about ±0.02V) after the LTO step. Also, as we hoped when we were designing the active probes, the circuit designs are quite robust to shifts in the threshold voltages. The next few figures show schematics for some of the circuit blocks along with measured test results after LTO. Figure 16 shows the current-voltage and conductance characteristics of the individual NMOS and PMOS transistors.

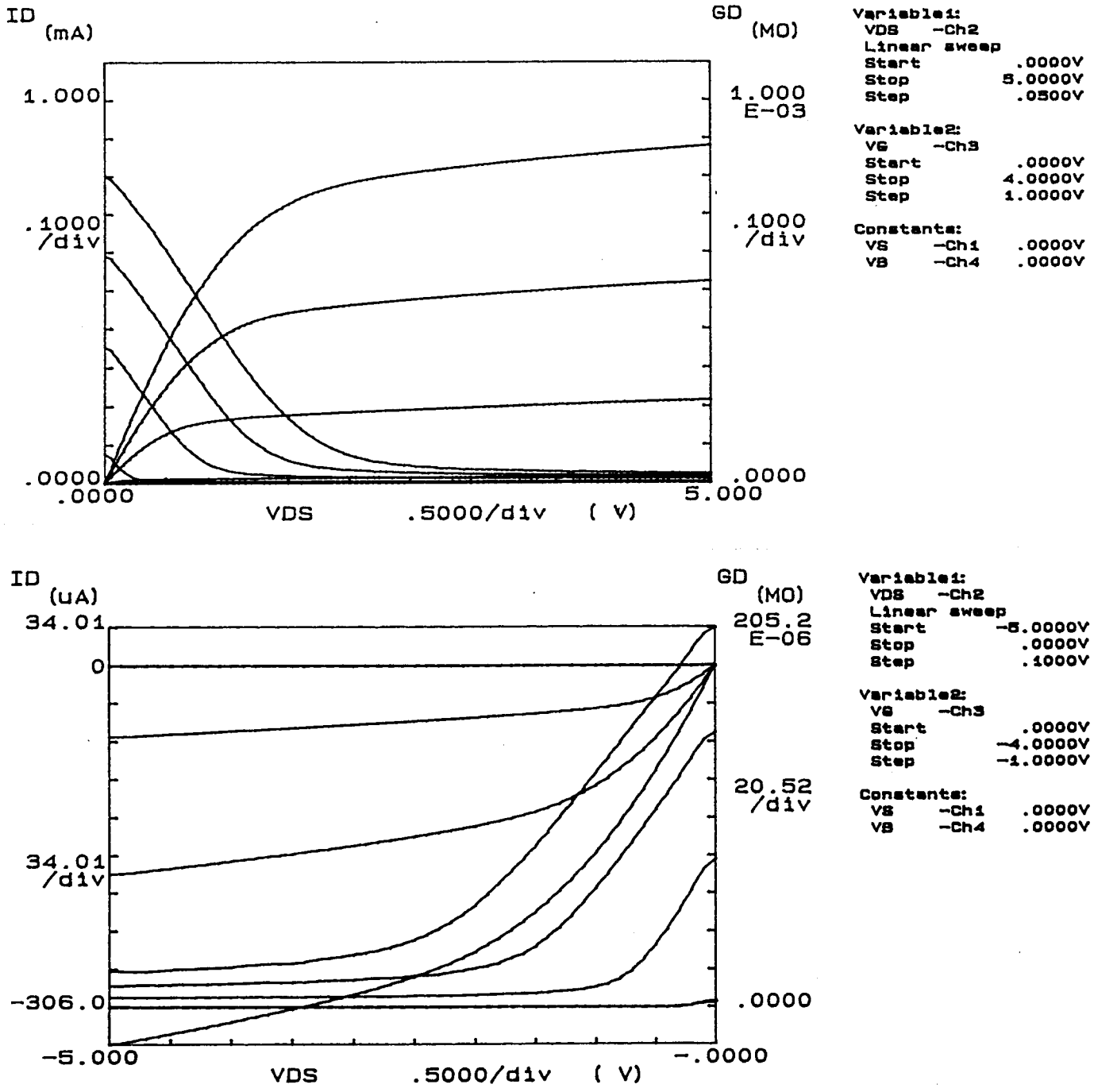


Fig. 16: The drain characteristics of the NMOS and PMOS transistors. (w/l=12μm/3μm)

Probe "BUF1" uses simple source followers as the output buffers. This is, hopefully, a "bullet proof" design because of its simplicity. Figure 17 shows the circuit schematic of this probe along with the measured input-output characteristics for a 1kHz input sine wave after final EDP. The gain of the buffer is around 0.85. This probe is ready for in-vivo testing. However, to obtain a very low output resistance in this design, the circuitry must consume a rather large area and significant power compared to some other designs. In order to reduce power/area consumption, the probe "BUF2," which has a push-pull type buffer, was designed. Its efficiency is four times higher than the source follower. However, because of its two stages, more signal is lost --- the gain of this type of buffer is typically around 0.65 as shown in Fig. 18.

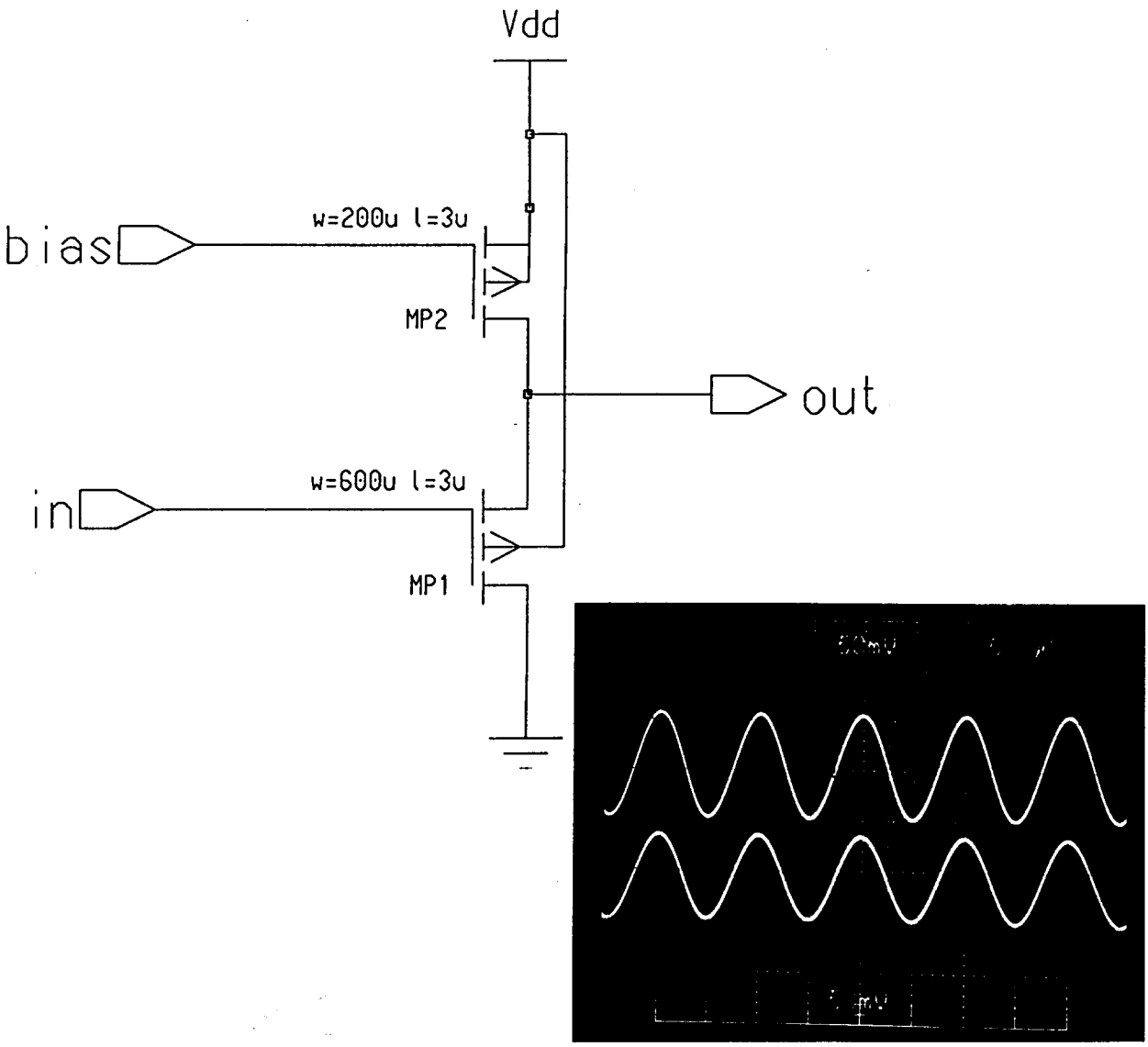


Fig. 17: A schematic of the source follower probe "BUF1" and measured input and output waveforms for a 1kHz input sine wave.

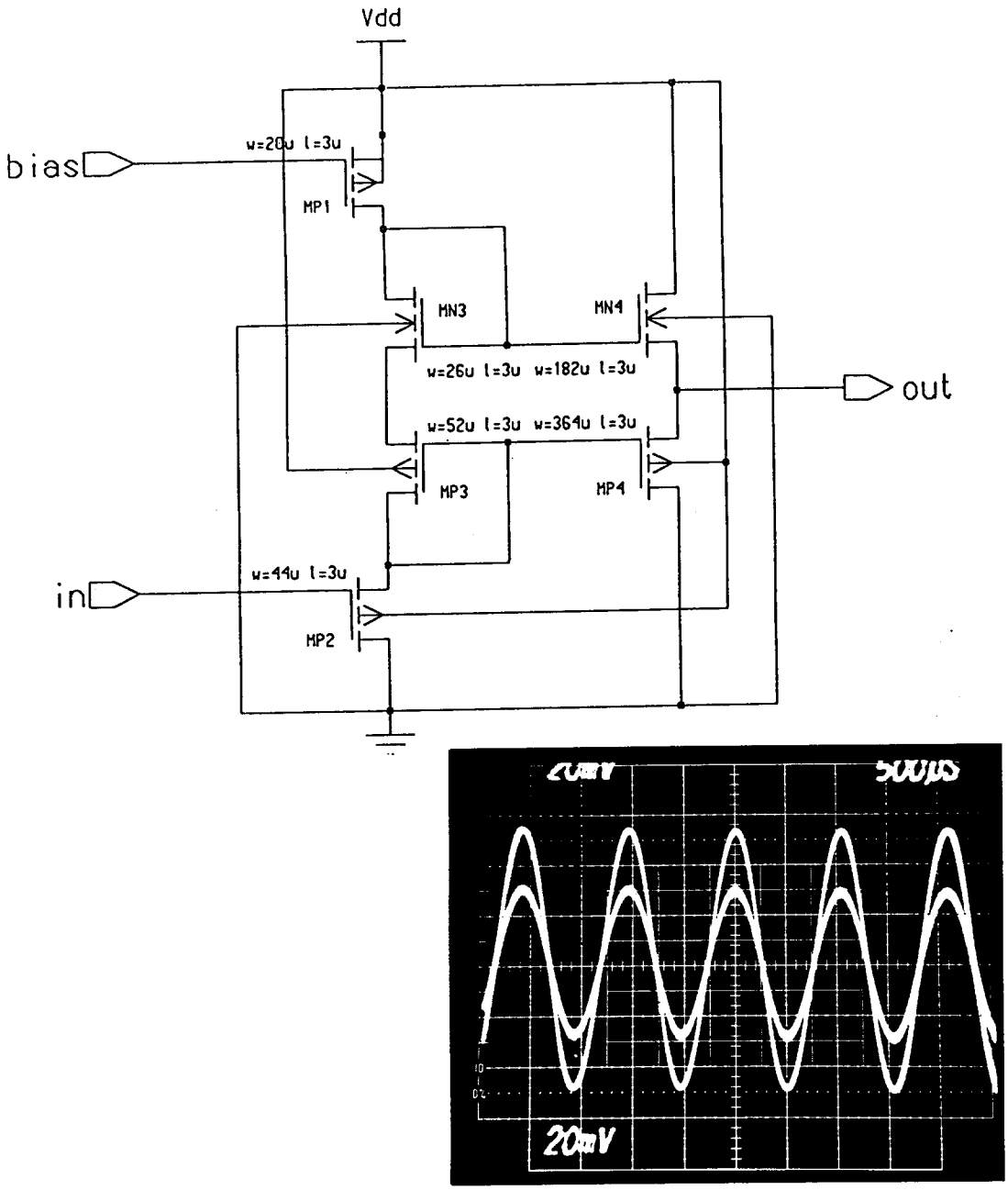


Fig. 18: Circuit schematic of the probe "BUF2" containing a two-stage open-loop buffer along with the measured input-output waveforms.

We have also designed a probe with an on-chip gain stage using a three-stage open loop amplifier. This is a somewhat more complicated design (Fig. 19), but it offers a gain of 50dB at 100Hz. These amplifiers "AMP1" are fully functional, although the measured bandwidth is a little narrower than the targeted value. Finally, the most complex of these designs realizes a unity-gain buffer using an opamp as shown in Fig. 20. This probe has advantages of unity-gain, low-power, and high power-supply noise rejection and is also fully functional. During the coming term, more of these various probes will be fabricated and will be tested in-vitro and in-vivo.

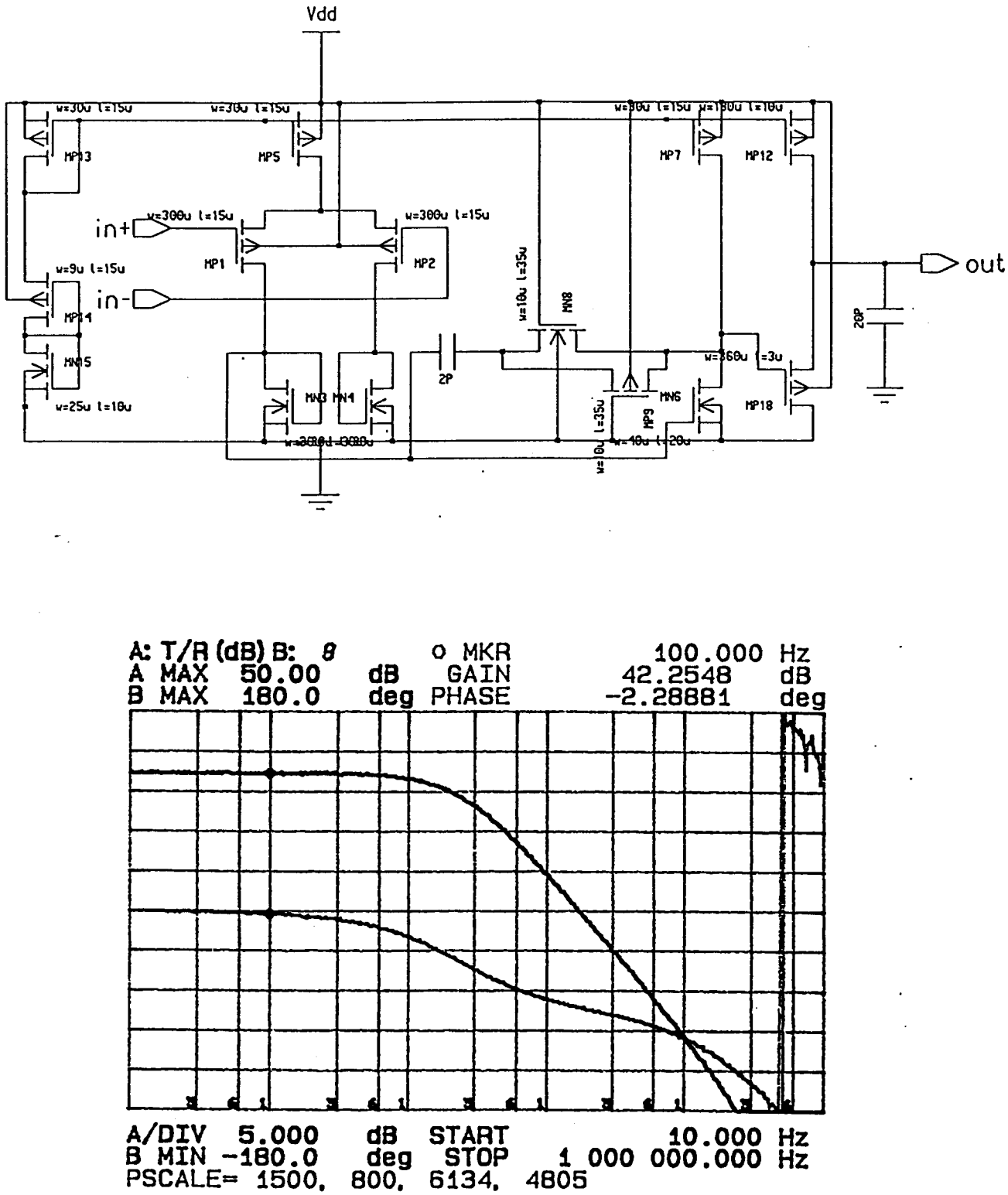


Fig. 19: Circuit schematic of a probe containing a push-pull amplifier along with the measured gain/phase-frequency plot. The low-frequency gain is 50dB with a bandwidth of about 5kHz. This active probe uses common recording site as one of the input nodes of the amplifier.

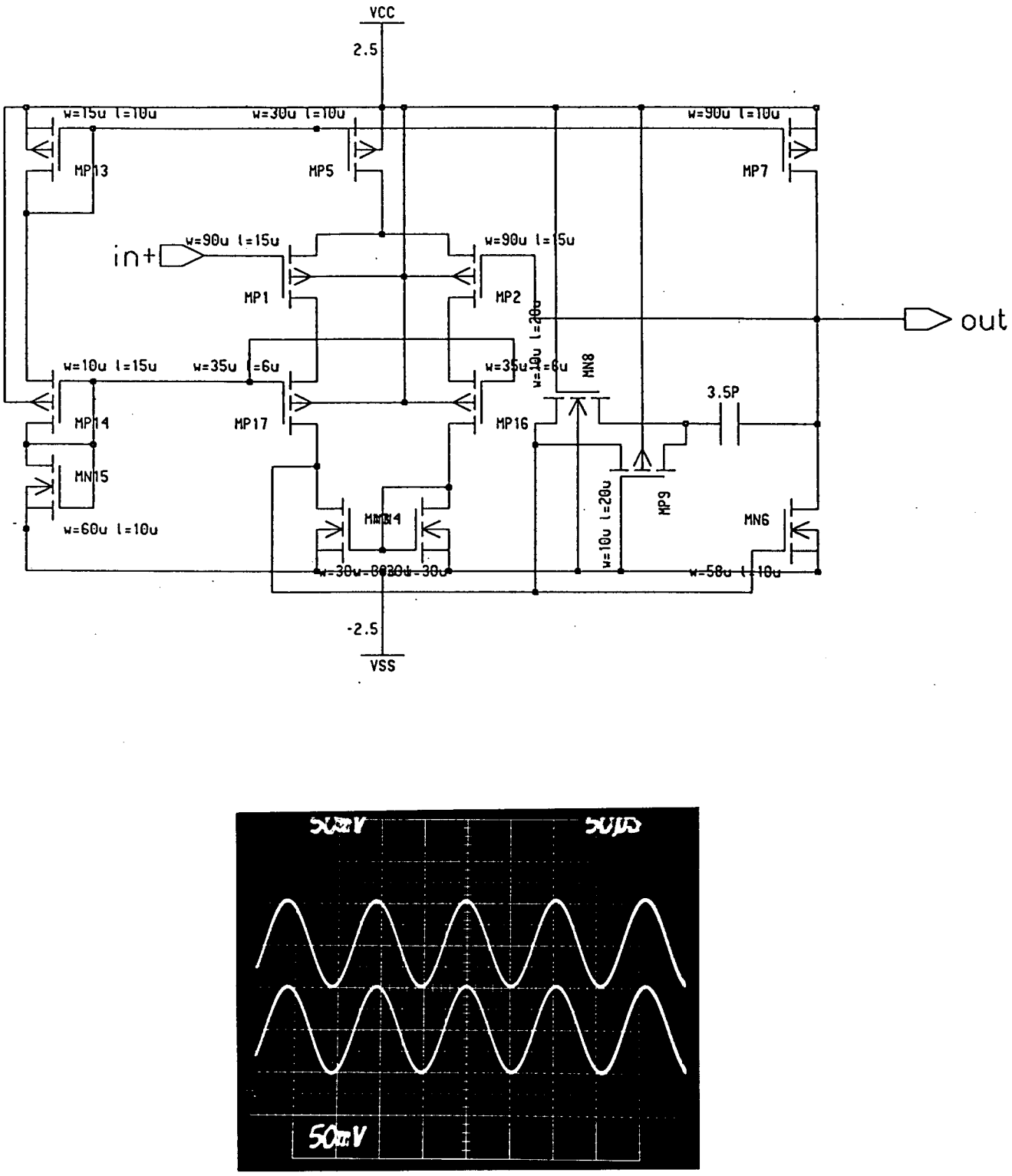


Fig. 20: A probe containing a unity-gain buffer realized using an operational amplifier and its input output waveforms.

4. *Conclusions*

As we have begun this new contract, we have focused our efforts on the development of high-yield active probe structures. We are examining four variations for the formation of Ir/Ti recording sites. The first is the self-aligned single-mask structure used originally. This structure produces a small site and maintains a simple process but does not allow cleaning of the site prior to metallization and is thus prone to problems with adhesion and electrical surface barriers. A second approach involves two masks, cutting through the upper portion of the encapsulating dielectric stack with a dry etch and then following this with a wet etch. The metal is inlayed using a second (larger) mask after an intermediate cleaning step to remove any polymer residue from the surface. This solves the polymer problems but the sidewall of the dielectric opening is irregular and can lead to step coverage problems. Finally, a third approach cuts through the upper dielectrics to the polysilicon interconnects with a dry etch, deposits the final oxide insulation (LTO), and then opens the contacts through this final layer with a wet etch and a smaller mask. This appears to overcome both the polymer and the step coverage problems and will be evaluated in a study to be conducted during the coming term. The goal is to realize reproducible sites that are free from all of the intermittent problems experienced in the past.

We are also focusing on the development of a series of active 2D and 3D probes as the forerunner of larger arrays to be developed under this contract. The present probes contain one and two-stage unity-gain buffers, amplifiers, multiplexers, and closed-loop "operational" amplifiers configured in a unity-gain mode. Problems associated with circuit contact resistances appear to have been overcome through work in process development. Metal-silicon contact resistances are now less than 5Ω for all contact combinations. The new probes have been successfully encapsulated using LTO films deposited in our laboratory and all designs have been found fully functional with circuit performance close to design targets. For active 3D structures, the problem of protecting the circuit areas from the final probe separation etch while allowing the shanks and 3D mounting "wings" to etch all the way down to the boron etch-stop is an important one. We have successfully used a back etch mask for this purpose, and working probes have been produced. During the coming term, we plan on completing the testing of these probes both in-vitro and in-vivo.